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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,635	09/04/2003	Huei-Pei Kuo	10007804-1	8116

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HEWLETT PACKARD COMPANY  
P O BOX 272400, 3404 E. HARMONY ROAD  
INTELLECTUAL PROPERTY ADMINISTRATION  
FORT COLLINS, CO 80527-2400

EXAMINER
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HU, SHOUXIANG

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/656,635

Applicant(s)

KUO ET AL.

Examiner

Shouxiang Hu

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) 5-10, 12, 17-22, 24 and 26-29 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 11, 13-15, 23 and 25 is/are rejected.
- 7) ☒ Claim(s) 4 and 16 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Election/Restrictions***

Claims 1-29 are pending in this application; and claims 1-4, 11, 13-16, 23 and 25 remain active in this office action, in view of the previous office action.

### ***Response to Declaration***

The declaration of Huei Pei Kuo filed on November 14, 2005 under 37 CFR 1.132 has been considered. And, it appears to be effective to overcome the prior art reference of Chen (US 2003/0143788 A1).

### ***Claim Objections***

Claims 1-4, 11, 13-16, 23 and 25 are objected to because of numerous informalities and/or defects, including but not limited to:

Claims 1, 11, 13, and 23 are incomplete for omitting essential steps, such omission amounting to a gap between the steps, which may make the claimed invention indefinite. The omitted steps are: the steps of forming and patterning the dielectric layer before forming the semiconductive or conductive surface. Otherwise, the recited electrical field could be generated through a variety of different methods that would not be readable on the instant invention. For example, it could be generated through an electrode having non-uniformly distributed surface charges and/or with reduced size

(e.g., smaller than the intended porous-forming region), and placed opposite to the semiconductor or conductor surface during the step of anodization.

Claims 1, 13, and 25 each need to clarify that the step of forming of the recited the semiconductive or conductive surface is actually the process step of forming a semiconductor or conductor layer that results in the recited surface.

Claim 1 recites the terms of “central area of a semi-conductive or conductive surface” and “a central area of the surface”, but fails to clarify what are the positional relationships between them. Claim 1 further recites the term of “the central area”, but fails to clarify which of the two central areas it definitely refers to.

Claim 2 recites the term of “central region”, but fails to clarify its positional relationship with the central areas recited in claim 1.

Claim 3 recites “further comprising the step of anodizing”, but there is only one step of anodizing in the instant invention, according to the instant disclosure.

In addition, claim 3 recites the term of “anodized region”, but fails to clarify its relationship with the porous region defined in claim 1.

In claims 4 and 16, the term of “the first conductive layer” lacks a sufficient antecedent basis in the claim.

Claim 14 recites the term of “central region”, but fails to clarify its positional relationship with the central area recited in claim 1.

Claim 15 recites “further comprising the step of anodizing”, but there is only one step of anodizing in the instant invention, according to the instant disclosure.

In addition, claim 15 recites the term of "anodized region", but fails to clarify its relationship with the pores defined in claim 1.

Claim 25 recites the term of "central region", but fails to clarify its positional relationship with the central area also recited in the claim.

Claim 25 needs to further clarify the meaning of "improved electron emission efficiency over an outer perimeter of the central region", as it is not definite about what is the second area/region with which the recited central area's emission efficiency is intended to compare.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 11, 13 and 23, as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 102(e) as being anticipated by Ichihara (Ichihara et al., EP 1094485 A2; of record).

Ichihara discloses a method for fabricating a porous flat electron emission device (Figs. 1-3; also see [0063-0066]), the method comprising: forming a semi-conductive flat emitter surface (of the silicon layer 3 in Fig. 2B) over a substrate (11); and, anodizing the semiconductive flat emitter surface which naturally forms porous region therein,

wherein the strength of the electric field generated during the anodizing step at a central area of the semi-conductive surface that is substantially away from the edges of layer 3 is naturally as great as the one at the perimeter of that central area, and naturally results in the anodization effects recited in the claims, since the electrical field at the surface of layer 3 (especially at the central area) is naturally substantially uniform during the step of anodizing, given that no dielectric layer is formed above the layer 3 to cause non-uniform distribution of the electric field during the anodizing step.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 11, 13-15, 23 and 25, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art ("AAPA") in view of Simon (Simon et al., US 3,699,404) and/or Sakemura (Sakemura et al., US 6,404,124).

AAPA disclose a method for fabricating a porous flat electron emission device (Figs. 1-6), the method comprising: forming a semi-conductive surface (14, of a silicon layer) over the substrate; anodizing the semi-conductive conductive surface; and, forming a dielectric layer/barrier (16) over a substrate (12) and forming an opening in the dielectric layer/barrier to expose a central region of an underlying layer.

Although AAPA does not expressly disclose that the dielectric layer can be formed prior to the formation of the semiconductive surface (or layer), one of ordinary skill in the art would readily recognize that the dielectric layer can be desirably formed first and in contact with the substrate for better defining the active region of the emitter, as evidenced in Simon (see the aperture-defining dielectric layer 13 in the cover pager figure) and/or Sakemura (see the aperture-defining dielectric layer 17 in Fig. 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to develop the method of AAPA with the steps of forming and patterning the dielectric layer being carried out prior to the step of forming the semiconductive surface, per the teachings of Simon and/or Sakemura, so that a method for forming a flat electron emitter with better defined active region would be obtained. And, with the collectively taught method, the strength of the electric field generated during the anodizing step at the central area of the semi-conductive surface corresponding to the opening of the dielectric layer would be naturally at least as great as the one at a perimeter of that central area/region in the anodized semi-conductor surface/layer as defined by the inner edge of the opening, since the semi-conductive surface/layer therein would have been formed above the dielectric layer and the substrate in a manner substantially same as the one in the elected species of the instant invention. And, it should result in an improvement in porous distributions therein substantially as that as in the instant invention.

***Allowable Subject Matter***

Claims 4 and 16 are further objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and to overcome the relevant claim objections set forth above in this Office action.

***Response to Arguments***

Applicant's arguments with respect to claims 1-4, 11, 13-16, 23 and 25 have been considered but are moot in view of the new ground(s) of rejection and/or objections.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH  
January 18, 2006



**SHOUXIANG HU**  
**PRIMARY EXAMINER**